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Applicant:	Michael Tayler, et al.
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APPELLANTS' BRIEF ON APPEAL

This is an appeal pursuant to 35 U.S.C. § 134 from the Examiner's decision rejecting claims 1-33 as set forth in the Final Office Action of January 29, 2007.

REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, L.P., a Texas Limited Partnership having its principal place of business in Houston, Texas.

RELATED APPEALS AND INTERFERENCES

Applicant's attorney knows of no related pending appeals or interferences.

STATUS OF CLAIMS

Claims 1-33 are pending in this application.

Claims 1-33 stand rejected and are the subject of this appeal. More specifically:

- claims 1-20, 23, and 27-33 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Bailey et al. (U.S. Pat. No. 5,012,435); and
- claims 21, 22, and 24-26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bailey et al. (U.S. Pat. No. 5,012,435) in view of Tamura et al. (U.S. Pat. No. 6,247,138).

STATUS OF AMENDMENTS

No after-final amendments have been filed in this case.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a device (FIG. 2, element 200; paragraph [0024]) comprising:

an overflow generator (FIG. 2, element 220; FIG. 3; paragraphs [0024]-[0033]) to generate a plurality of overflow signals having a plurality of periods (FIGS. 2 and 3, elements 224a-d; paragraphs [0024]-[0033]);

a plurality of control registers (FIG. 2, elements 232 and 234a-234t; paragraphs [0024]-[0038]) storing a plurality of selection values (paragraphs [0034]-[0042]); and

a first trigger generator (FIG. 2, element 204a; paragraphs [0024], [0034]-[0042]) comprising first trigger generation means for generating a first timeout event trigger signal based on the plurality of overflow signals and a first one of the plurality of selection values (FIG. 4, element 400; paragraphs [0043]-[0047]; FIG. 5, element 500; paragraphs [0048]-[0053]).

Independent claim 10 is directed to a device comprising:

an overflow generator (FIG. 2, element 220; FIG. 3; paragraphs [0024]-[0033]) to generate a plurality of overflow signals having a plurality of periods (FIGS. 2 and 3, elements 224a-d; paragraphs [0024]-[0033]);

a plurality of control registers (FIG. 2, elements 232 and 234a-234t; paragraphs [0024]-[0038]) storing a plurality of selection values and a plurality of control values (paragraphs [0034]-[0042]);

a first trigger generator (FIG. 2, element 204a; paragraphs [0024], [0034]-[0042]) comprising first trigger generation means for generating a first timeout event trigger signal based on the plurality of overflow signals, a first one of the plurality of selection values, and a first one of the plurality of control values (FIG. 4, element 400; paragraphs [0043]-[0047]; FIG. 5, element 500; paragraphs [0048]-[0053]); and

a second trigger generator (FIG. 2, element 204*t*; paragraphs [0024], [0034]-[0042]) comprising second trigger generation means for generating a second timeout event trigger signal based on the plurality of overflow signals, a second one of the plurality of selection values, and a second one of the plurality of control values(FIG. 4, element 400; paragraphs [0043]-[0047]; FIG. 5, element 500; paragraphs [0048]-[0053]).

Independent claim 11 is directed to a method (FIG. 6, element 600) comprising steps of:

(A) generating a plurality of overflow signals having a plurality of periods (FIG. 6, element 602; paragraph [0039]);

(B) generating plurality of selection values (FIG. 6, element 606; paragraph [0040]); and

(C) generating a first timeout event trigger signal based on the plurality of overflow signals and a first one of the plurality of selection values (FIG. 6, element 608; paragraph [0041]).

Independent claim 20 is directed to a method (FIG. 6, element 600) comprising steps of:

(A) generating a plurality of overflow signals having a plurality of periods (FIG. 6, element 602; paragraph [0039]);

(B) generating plurality of selection values (FIG. 6, element 606; paragraph [0040]);

(C) generating a plurality of control values (FIG. 6, element 604; paragraph [0040]);

(D) generating a first timeout event trigger signal based on the plurality of overflow signals, a first one of the plurality of selection values, and a first one of the plurality of control values (FIG. 6, element 608; paragraph [0041]); and

(E) generating a second timeout event trigger signal based on the plurality of overflow signals, a second one of the plurality of selection values, and a second one of the plurality of control values (FIG. 6, element 610; paragraph [0042]).

Independent claim 21 is directed to a device (FIG. 4, element 400; paragraphs [0043]-[0047]) comprising:

a multiplexer (FIG. 4, element 402) comprising a plurality of data inputs (FIG. 4, elements 412a-d) to receive a plurality of overflow signals (FIG. 4, elements 224a-d), a selection input (FIG. 4, elements 410a-b) to receive a selection signal (FIG. 4, elements 226a-b), and an output (FIG. 4, element 414) to provide one of the plurality of overflow signals selected by the selection signal (paragraphs [0043]-[0047]);

a one-bit counter (FIG. 4, element 404; paragraphs [0044]-[0045]), comprising a data input (FIG. 4, element 416b) coupled to the output of the multiplexer, a reset input (FIG. 4, element 416c), and a data output (FIG. 4, element 418) to provide a one-bit count signal (paragraphs [0044]-[0045]); and

an AND gate (FIG. 4, element 406) having a first input (FIG. 4, element 420a) coupled to the data output of the one-bit counter, a second input (FIG. 4, element 420b) coupled to the output of the multiplexer, and an output (FIG. 4, element 422) to provide a first timeout event trigger signal (paragraphs [0046]-[0047]).

Independent claim 23 is directed to a device (FIG. 4, element 400; paragraphs [0043]-[0047]) comprising:

selection means (FIG. 4, element 402) comprising means for receiving a plurality of overflow signals (FIG. 4, elements 412a-d), means for receiving a selection signal (FIG. 4, elements 410a-b), means for selecting one of the plurality of overflow signals based on the selection signal (FIG. 4, element 402), and means for providing as output the selected one of the plurality of overflow signals (FIG. 4, element 414, paragraphs [0043]-[0047]);

counting means (FIG. 4, element 404; paragraphs [0044]-[0045]) for counting the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event (paragraphs [0044]-[0045]); and

timeout event trigger signal generation means (FIG. 4, element 406) for asserting a timeout event trigger signal when the selected one of the plurality of overflow signals has been asserted twice since the predetermined reset event (paragraphs [0046]-[0047]).

Independent claim 25 is directed to a device (FIG. 5, element 500; paragraphs [0048]-[0053]) comprising:

a multiplexer (FIG. 5, element 502) comprising a plurality of data inputs (FIG. 5, elements 512a-d) to receive a plurality of overflow signals (FIG. 5, elements 224a-d), a selection input (FIG. 5, elements 510a-b) to receive a selection signal (FIG. 5, elements 226a-b), and an output (FIG. 5, element 514) to provide one of the plurality of overflow signals selected by the selection signal (paragraphs [0048]-[0053]);

a multi-bit counter (FIG. 5, element 504; paragraphs [0049]-[0050]); comprising a data input (FIG. 5, element 516b) coupled to the output of the multiplexer, a reset input (FIG. 5, element R inside 504), and a plurality of data outputs to provide a multi-bit count signal (FIG. 5, elements 530a-*n*; paragraphs [0048]-[0053]);

a multi-bit comparator (FIG. 5, element 528) having a first plurality of inputs (FIG. 5, elements 534a-*n*) coupled to the plurality of data outputs of the multi-bit counter, a second plurality of inputs (FIG. 5, elements 532a-*n*) to receive a multi-bit control signal, and a data output (FIG. 5, element 536) to provide a

comparison signal indicating whether the multi-bit count signal is equal to the multi-bit control signal (paragraphs [0048]-[0053]); and

an AND gate (FIG. 5, element 506) having a first input (FIG. 5, element 520a) coupled to the data output of the multi-bit comparator, a second input (FIG. 5, element 520b) coupled to the output of the multiplexer, and an output (FIG. 5, element 522) to provide a first timeout event trigger signal.

Independent claim 27 is directed to a device (FIG. 5, element 500; paragraphs [0048]-[0053]) comprising:

selection means (FIG. 5, element 502) comprising means for receiving a plurality of overflow signals (FIG. 5, elements 512a-d), 224a-d, means for receiving a selection signal (FIG. 5, elements 510a-b), means for selecting one of the plurality of overflow signals based on the selection signal (FIG. 5, element 502), and means for providing as output the selected one of the plurality of overflow signals (FIG. 5, element 514, paragraphs [0048]-[0053]);

counting means (FIG. 5, element 504) for counting the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event (paragraphs [0048]-[0053]);

comparison means (FIG. 5, element 528) for generating a comparison signal indicating whether a predetermined control value is at least equal to the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event (paragraphs [0048]-[0053]); and

timeout event trigger signal generation means (FIG. 5, element 506) for asserting a timeout event trigger signal when the predetermined control value is at least equal to the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event.

Independent claim 29 is directed to a method comprising steps of:

(A) receiving a plurality of overflow signals having a plurality of periods (FIG. 7, element 702; paragraph [0054]);
(B) receiving a first selection signal (FIG. 7, element 704; paragraph [0054]);
(C) identifying a first one of the plurality of overflow signals based on the first selection signal (FIG. 7, element 706; paragraph [0055]); and

(D) generating a first trigger signal based on the identified one of the plurality of overflow signals (FIG. 7, element 708; paragraph [0055]).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection for review are:

(1) the rejection of claims 1-20, 23, and 27-33 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Bailey et al. (U.S. Pat. No. 5,012,435); and

(2) the rejection of claims 21, 22, and 24-26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bailey et al. (U.S. Pat. No. 5,012,435) in view of Tamura et al. (U.S. Pat. No. 6,247,138).

ARGUMENT

Rejection of Claims 1-20, 23, and 27-33 under 35 U.S.C. § 102(b) (Bailey)

Claims 1-20, 23, and 27-33 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Bailey et al. (U.S. Pat. No. 5,012,435). More specifically, the Office Action asserts that "a plurality of overflow signals" reads on elements 552A-C in FIG. 8 of

Bailey;[1] that "a plurality of periods" reads on FIGS. 6A-6B of Bailey; that "a plurality of control registers storing a plurality of selection values" reads on elements 510a-c in FIG. 8 of Bailey; and that "a first trigger generator comprising first trigger generation means for generating a first timeout event trigger signal based on the plurality of overflow signals and a first one of the plurality of selection values" reads on FIG. 2 of Bailey.

Applicant disagrees with this interpretation of Bailey and respectfully traverses this rejection. Claim 1 of the present application expressly recites "an overflow generator to generate a plurality of overflow signals having a plurality of periods." Although the Office Action states that signals 552A-C in FIG. 8 of Bailey read on such overflow signals, they do not, because Bailey does not disclose that the signals 552A-C are periodic, i.e., that they "hav[e] a plurality of periods," as expressly required by claim 1.

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[1] Although the Office Action refers at some points to signals 522A-C and at some points to signals 552A-C, it is assumed herein that all of these references are intended to refer to signals 552A-C, since the Office Action refers to these signals as the outputs of the comparators 550A-C, which have output signals 552A-C. This confusion may stem from the fact that in FIG. 8 of Bailey, signal 552C is mistakenly labeled as "522C," resulting in two signals in FIG. 8 being labeled as signal "522C."

The Office Action does not point to any teaching in Bailey that the signals 552A-C are periodic, i.e., that they "hav[e] a plurality of periods," as expressly required by claim 1. Instead, the Office Action merely asserts, without any evidence, that "Bailey discloses a plurality of overflow signals (Fig. 8, elements 552A-C) . . . [which are] outputs of the comparators, which are then provided to timeout logic 560 and also provided to event logic 580." (Office Action, p.15). This assertion does not indicate how Bailey teaches that the signals 552A-C are periodic.

The Office Action also asserts that the "timer circuit [of Bailey] has the capability to monitor a multiple of timeout periods and provide either a general single timeout signal or a specific timeout signal upon the occurrence of each timeout period." (Office Action, p.16.) Even if this assertion is assumed to be true for purposes of argument, it is irrelevant because it does not correspond to the actual express limitations of claim 1 of the present application. Claim 1 does not claim generally "a timer circuit [which] has the capability to monitor a multiple of timeout periods." Rather, claim 1 expressly recites a plurality of overflow *signals* having a plurality of periods. The Office Action does not point to any teaching in Bailey of such signals or of "an overflow generator to generate" such signals, as expressly required by claim 1.

Rather, Bailey discloses that the signals 552A-C in FIG. 8 are generated by the comparators 550A-C, respectively, in response to comparisons of the counter signal 532 to the outputs of the registers 510A-510C, respectively. Taking comparator 550A as an example, the signal 552A output by comparator 552A will vary depending on the value of the counter signal 532 and the time at which the load signal 522A was last asserted. (See Bailey, col. 7, lies 15-63.) Bailey does not disclose, and gives no basis for concluding, that the load signal 522A is periodic, that the signal output by the register 510A at 516A is periodic, or that the resulting output of the comparator 552A is periodic. Therefore Bailey neither discloses nor gives any basis for concuding that any of these signals are periodic. Therefore none of them is an "overflow signal" as expressly recited by claim 1.

The Office Action, therefore, fails to demonstrate that Bailey teaches an express limitation of claim 1. Claim 1, therefore, patentably distinguishes over Bailey, and the rejection of claim 1 over Bailey should be reversed.

Claims 2-7 depend, either directly or indirectly, from claim 1 and therefore patentably distinguish over Bailey for at least the same reasons.

Independent claim 10 includes the same relevant limitations as claim 1 and therefore patentably distinguishes over Bailey for at

least the same reasons. Claims 11-19 depend, either directly or indirectly, from claim 10 and therefore patentably distinguish over Bailey for at least the same reasons.

Independent claim 20 includes the same relevant limitations as claim 1 and therefore patentably distinguishes over Bailey for at least the same reasons.

Applicant traverses the rejection of independent claim 23 for similar reasons. In particular, the Office Action states that elements 61-64 of FIG. 1 in Bailey read on the "selection means comprising means for receiving a plurality of overflow signals" in claim 23, that FIG. 2 reads on "means for receiving a selection signal" and "means for selecting one of the plurality of overflow signals based on the selection signal," and that elements 522A-C of FIG. 8 read on "means for providing as output the selected one of the plurality of overflow signals."

The Office Action misinterprets Bailey. The plurality of "periods" shown in FIG. 5 of Bailey, for example, are not a plurality of periods *of a plurality of overflow signals*. The Office Action interprets signals 61-64 in FIG. 1 of Bailey as the "plurality of overflow signals." The "periods" shown in FIG. 5 are not the periods of signals 61-64 of FIG. 1. Rather, the "periods" shown in FIG. 5 are merely successive values of the *clock signal* output by the clock 40 (col. 5, lines 37-40). The Office Action

fails to point to any correlation between these "periods" and the periods of the signals 61-64 output by the timer output logic 60. Furthermore, the Office Action fails to point to any teaching in Bailey that the signals 61-64 are periodic (i.e., have periods).

Furthermore, the Office Action fails to point to any teaching in Bailey that signals 61-64 are "overflow" signals, as expressly required by claim 23. For example, the Office Action fails to point to any teaching that signals 61-64 are generated as the result of the overflow of a counter as shown, for example, in FIG. 3 of the present application.

Because claim 23 expressly recites "a plurality of overflow signals" and Bailey fails to disclose any "overflow signals," claim 23 patentably distinguishes over Bailey.

Furthermore, claim 23 recites "means for receiving a plurality of overflow signals." Although the Office Action cites signals 61-64 as "overflow signals," the overflow signals 61-64 in FIG. 1 of Bailey are the final output of the system shown in FIG. 1, and are not received by any other component of the system. Bailey, in other words, fails to disclose "means for receiving" the signals 61-64. Therefore, even if it were assumed for purposes of argument that the signals 61-64 were "overflow signals" within the meaning of claim 23, Bailey still fails to disclose an express element of claim 23. Claim 23, therefore, patentably distinguishes over Bailey.

Independent claim 27 includes the same relevant limitations as claim 23 and therefore patentably distinguishes over Bailey for at least the same reasons. Claim 28 depends from claim 27 and therefore patentably distinguishes over Bailey for at least the same reasons.

Independent claim 29 includes the same relevant limitations as claim 23 and therefore patentably distinguishes over Bailey for at least the same reasons. Claims 30-33 depend, either directly or indirectly, from claim 29 and therefore patentably distinguish over Bailey for at least the same reasons.

In conclusion, the rejection of claims 1-20, 23, and 27-33 is unfounded and should be reversed.

Rejection of Claims 21, 22, and 24-26 under 35 U.S.C. § 103(a) (Bailey in view of Tamura)

Claims 21, 22, and 24-26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bailey in view of Tamura et al. (U.S. Pat. No. 6,247,138).

Applicant traverses the rejection of claims 21, 22, and 24-26 for the same reasons provided above. Claim 21 includes substantially the same relevant limitation as claim 23, namely "a multiplexer comprising a plurality of data inputs to receive a plurality of overflow signals." As described above, the Office

Action points to no teaching or suggestion in Bailey of this express limitation. The Office Action does not assert that Tamura teaches or suggests this limitation. The combination of Bailey and Tamura, therefore, fails to teach or suggest this limitation of claim 21. Claim 22 depends from claim 21 and therefore patentably distinguishes over the combination of Bailey and Tamura for at least the same reason.

Claim 24, as amended, depends from claim 23 and therefore patentably distinguishes over the combination of Bailey and Tamura for at least the same reasons provided above with respect to claim 23.

Claim 25 includes the same relevant limitations as claim 21 and therefore patentably distinguishes over the combination of Bailey and Tamura for at least the same reasons. Claim 26 depends from claim 25 and therefore patentably distinguishes over the combination of Bailey and Tamura for at least the same reasons.

CONCLUSIONS

The Examiner's rejections of claims 1-33 should be reversed for the reasons stated above.

If this Brief is not considered timely filed and if a request for extension of time is otherwise absent, applicant hereby requests any extension of time. Please charge any fees or make any credits, to Deposit Account No. 08-2025.

Respectfully submitted,

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APPENDIX A: CLAIMS ON APPEAL

Claim 1. A device comprising:

an overflow generator to generate a plurality of overflow signals having a plurality of periods;

a plurality of control registers storing a plurality of selection values; and

a first trigger generator comprising first trigger generation means for generating a first timeout event trigger signal based on the plurality of overflow signals and a first one of the plurality of selection values.

Claim 2. The device of claim 1, wherein the plurality of control registers further stores a plurality of control values, and wherein the first trigger generation means comprises means for generating the first timeout event trigger signal based on the plurality of overflow signals, the first one of the plurality of selection values, and a first one of the plurality of control values.

Claim 3. The device of claim 1, further comprising:

a second trigger generator comprising second trigger generation means for generating a second timeout event trigger signal based on the plurality of overflow signals and a second one of the plurality of selection values.

Claim 4. The device of claim 3, wherein the plurality of control registers further stores a plurality of control values, and wherein the second trigger generation means comprises means for generating the second timeout event trigger signal based on the plurality of overflow signals, the second one of the plurality of selection values, and a second one of the plurality of control values.

Claim 5. The device of claim 1, wherein the first trigger generation means comprises:

means for identifying a first one of the plurality of overflow signals based on the first one of the plurality of selection signals;

means for identifying a period of the first one of the plurality of overflow signals; and

means for generating the first timeout event trigger signal based on the period of the first one of the plurality of overflow signals.

Claim 6. The device of claim 1, wherein the means for generating the first timeout event trigger signal based on the period of the first one of the plurality of overflow signals comprises means for asserting the first timeout event trigger signal if the period of the first one of the plurality of overflow signals has elapsed since the first trigger generator was last reset.

Claim 7. The device of claim 1, wherein the plurality of control registers further stores a plurality of control values, and wherein the first trigger generation means comprises:

means for identifying a first one of the plurality of overflow signals based on the first one of the plurality of selection signals; and

means for generating the first timeout event trigger signal based on the first one of the plurality of overflow signals and a first one of the plurality of control signals.

Claim 8. The device of claim 7, wherein *C* is the first one of the plurality of control values, and wherein the means for generating the first timeout event trigger signal based on the first one of the plurality of overflow signals and a first one of the plurality of control signals comprises:

means for asserting the first timeout event trigger signal if the first one of the plurality of overflow signals has been asserted at least *C*+1 times since a first predetermined reset event; and

means for deasserting the first timeout event trigger signal otherwise.

Claim 9. The device of claim 7, wherein *C* is the first one of the plurality of control values, wherein *P* is the period of the first one of the plurality of overflow signals, and wherein the means for generating the first timeout event trigger signal based on the first one of the plurality of overflow signals and a first one of the plurality of control signals comprises:

means for asserting the first timeout event trigger signal if an amount of time at least equal to *PC* has elapsed since a predetermined reset event; and

means for deasserting the first timeout event trigger signal otherwise.

Claim 10. A device comprising:

an overflow generator to generate a plurality of overflow signals having a plurality of periods;

a plurality of control registers storing a plurality of selection values and a plurality of control values;

a first trigger generator comprising first trigger generation means for generating a first timeout event trigger signal based on the plurality of overflow signals, a first one of the plurality of selection values, and a first one of the plurality of control values; and

a second trigger generator comprising second trigger generation means for generating a second timeout event trigger signal based on the plurality of overflow signals, a second one of the plurality of selection values, and a second one of the plurality of control values.

Claim 11. A method comprising steps of:

(D) generating a plurality of overflow signals having a plurality of periods;

(E) generating plurality of selection values; and

(F) generating a first timeout event trigger signal based on the plurality of overflow signals and a first one of the plurality of selection values.

Claim 12. The method of claim 11, further comprising a step of:

(G) generating a plurality of control values; and

wherein the step (C) comprises a step of generating the first timeout event trigger signal based on the plurality of overflow signals, the first one of the plurality of selection values, and a first one of the plurality of control values.

Claim 13. The method of claim 11, further comprising a step of:

(D) generating a second timeout event trigger signal based on the plurality of overflow signals and a second one of the plurality of selection values.

Claim 14. The method of claim 13, further comprising a step of:

(E) generating a plurality of control values; and

wherein the step (D) comprises a step of generating the second timeout event trigger signal based on the plurality of overflow signals, the second one of the plurality of selection values, and a second one of the plurality of control values.

Claim 15. The method of claim 11, wherein the step (C) comprises steps of:

(C)(1) identifying a first one of the plurality of overflow signals based on the first one of the plurality of selection signals;

(C)(2) identifying a period of the first one of the plurality of overflow signals; and

(C)(3) generating the first timeout event trigger signal based on the period of the first one of the plurality of overflow signals.

Claim 16. The method of claim 15, wherein the step (C)(3) comprises a step of asserting the first timeout event trigger signal if the period of the first one of the plurality of overflow signals has elapsed since a first predetermined reset event.

Claim 17. The method of claim 11, further comprising a step of:

(D) generating a plurality of control values; and

wherein the step (C) comprises steps of:

(C)(1) identifying a first one of the plurality of overflow signals based on the first one of the plurality of selection signals; and

(C)(2) generating the first timeout event trigger signal based on the first one of the plurality of overflow signals and a first one of the plurality of control signals.

Claim 18. The method of claim 17, wherein the first one of the plurality of control signals represents a value *C*, and wherein the step (C)(2) comprises steps of:

(C)(2)(1) asserting the first timeout event trigger signal if the first one of the plurality of overflow signals has been asserted at least (*C*+1) times since a first predetermined reset event; and

(C)(2)(2) deasserting the first timeout event trigger signal otherwise.

Claim 19. The method of claim 17, wherein the first one of the plurality of control signals represents a value *C*, wherein *P* is the period of the first one of the plurality of overflow signals, and wherein the step (C)(2) comprises steps of:

(C)(2)(1) asserting the first timeout event trigger signal if an amount of time at least equal to *PC* has elapsed since a predetermined reset event; and

(C)(2)(2) deasserting the first timeout event trigger signal otherwise.

Claim 20. A method comprising steps of:

(F) generating a plurality of overflow signals having a plurality of periods;

(G) generating plurality of selection values;

(H) generating a plurality of control values;

(I) generating a first timeout event trigger signal based on the plurality of overflow signals, a first one of the plurality of selection values, and a first one of the plurality of control values; and

(J) generating a second timeout event trigger signal based on the plurality of overflow signals, a second one of the plurality of selection values, and a second one of the plurality of control values.

Claim 21. A device comprising:

a multiplexer comprising a plurality of data inputs to receive a plurality of overflow signals, a selection input to receive a selection signal, and an output to provide one of the plurality of overflow signals selected by the selection signal;

a one-bit counter comprising a data input coupled to the output of the multiplexer, a reset input, and a data output to provide a one-bit count signal; and

an AND gate having a first input coupled to the data output of the one-bit counter, a second input coupled to the output of the multiplexer, and an output to provide a first timeout event trigger signal.

Claim 22. The device of claim 21, further comprising:

a latch comprising a data input coupled to the output of the AND gate, and an output to provide a second timeout event trigger signal.

Claim 23. A device comprising:

selection means comprising means for receiving a plurality of overflow signals, means for receiving a selection signal, means for selecting one of the plurality of overflow signals based on the selection signal, and means for providing as output the selected one of the plurality of overflow signals;

counting means for counting the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event; and

timeout event trigger signal generation means for asserting a timeout event trigger signal when the selected one of the plurality of overflow signals has been asserted twice since the predetermined reset event.

Claim 24. The device of claim 23, further comprising:

a latch comprising means for receiving a clock signal, means for receiving the first timeout event trigger signal, and means for providing the timeout event trigger signal as output in response to a transition in the clock signal.

Claim 25. A device comprising:

a multiplexer comprising a plurality of data inputs to receive a plurality of overflow signals, a selection input to receive a selection signal, and an output to provide one of the plurality of overflow signals selected by the selection signal;

a multi-bit counter comprising a data input coupled to the output of the multiplexer, a reset input, and a plurality of data outputs to provide a multi-bit count signal;

a multi-bit comparator having a first plurality of inputs coupled to the plurality of data outputs of the multi-bit counter, a second plurality of inputs to receive a multi-bit control signal, and a data output to provide a comparison signal indicating whether the multi-bit count signal is equal to the multi-bit control signal; and

an AND gate having a first input coupled to the data output of the multi-bit comparator, a second input coupled to the output of the multiplexer, and an output to provide a first timeout event trigger signal.

Claim 26. The device of claim 25, further comprising:

a latch comprising a data input coupled to the output of the AND gate, and an output to provide a second timeout event trigger signal.

Claim 27. A device comprising:

selection means comprising means for receiving a plurality of overflow signals, means for receiving a selection signal, means for selecting one of the plurality of overflow signals based on the selection signal, and means for providing as output the selected one of the plurality of overflow signals;

counting means for counting the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event;

comparison means for generating a comparison signal indicating whether a predetermined control value is at least equal to the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event; and

timeout event trigger signal generation means for asserting a timeout event trigger signal when the predetermined control value is at least equal to the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event.

Claim 28. The device of claim 27, further comprising:

a latch comprising means for receiving a clock signal, means for receiving the first timeout event trigger signal, and means for providing the timeout event trigger signal as output in response to a transition in the clock signal.

Claim 29. A method comprising steps of:

(E) receiving a plurality of overflow signals having a plurality of periods;
(F) receiving a first selection signal;
(G) identifying a first one of the plurality of overflow signals based on the first selection signal; and
(H) generating a first trigger signal based on the identified one of the plurality of overflow signals.

Claim 30. The method of claim 29, wherein the step (D) comprises a step of asserting the first timeout event trigger signal if an amount of time at least equal to the period of the first one of the plurality of overflow signals has elapsed since a first predetermined reset event.

Claim 31. The method of claim 29, further comprising a step of:

(I) receiving a first control signal; and

wherein the step (D) comprises a step of generating the first trigger signal based on the first control signal and the identified one of the plurality of overflow signals.

Claim 32. The method of claim 31, wherein the first one of the plurality of control signals represents a value *C*, and wherein the step (D) comprises steps of:

(D)(1) asserting the first timeout event trigger signal if the first one of the plurality of overflow signals has been asserted at least *C*+1 times since a first predetermined reset event; and

(D)(2) deasserting the first timeout event trigger signal otherwise.

Claim 33. The method of claim 31, wherein the first one of the plurality of control signals represents a value *C*, wherein *P* is the period of the first one of the plurality of overflow signals, and wherein the step (D) comprises steps of:

(D)(1) asserting the first timeout event trigger signal if an amount of time at least equal to *PC* has elapsed since a predetermined reset event; and

(D)(2) deasserting the first timeout event trigger signal otherwise.

APPENDIX B: EVIDENCE

No evidence is submitted in support of this Appeal Brief.

APPENDIX C: RELATED PROCEEDINGS

Applicant's attorney knows of no related pending appeals or interferences.